

MANUFACTURING TEST REQUIREMENT

PA-1650-41LS

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MODEL	REV	Written By	LITE-ON Electronics, Inc.
PA-1650-41LS	A	Joe Liao	SHEET 1 of 13

Revision History

REV. NO.	ITEM	DESCRIPTIONS OF CHANGE		CHANGED DATE :	REF. DOC. NO.
		BEFORE	AFTER		
X01			INITIAL	2020/11/18	
A			Released	2020/12/03	

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1. Input / Output Requirement

	MINIMUM	MAXIMUM	NORMAL(RATED)	Input Frequency
LOW RANGE	90VAC	137VAC	100~127VAC	50+/-3Hz
HIGH RANGE	180VAC	265VAC	200~240VAC	60+/-3Hz

DC Output	MIN	MAX	UNIT
20V	0	3.25	A
15V	0	3	A
9V	0	3	A
5V	0	3	A

2. Detail Description:

2.1. Inrush Current

20V output condition:

Test condition			Design Requirement
AC input	DC output		
100V/60Hz	+20V	3.25A	No component damage
240V/50Hz			No component damage

15V output condition:

Test condition			Design Requirement
AC input	DC output		
100V/60Hz	+15V	3A	No component damage
240V/50Hz			No component damage

9V output condition:

Test condition			Design Requirement
AC input	DC output		
100V/60Hz	+9V	3A	No component damage
240V/50Hz			No component damage

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5V output condition:

Test condition			Design Requirement
AC input	DC output		
100V/60Hz	+5V	3A	No component damage
240V/50Hz			No component damage

2.2. Rated Current

Test condition			Design Requirement
AC input	DC output		
90V/47Hz	+20V	3.25A	1.8A(max)
90V/47Hz	+15V	3A	1.8A(max)
90V/47Hz	+9V	3A	1.8A(max)
90V/47Hz	+5V	3A	1.8A(max)

2.3. Power Factor

Test condition			Design Requirement
AC input	DC output		
240V/50Hz	+20V	3.25A	REF

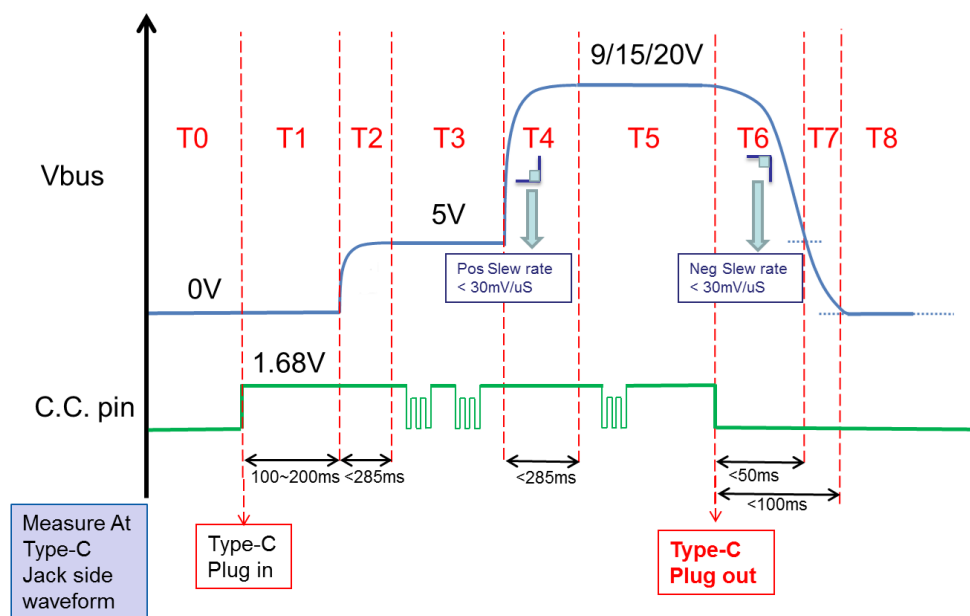
2.4. Turn-On Time

Test condition			Design Requirement
AC input	DC output		
100V/60Hz	+20V	3.25A	3 sec.(max)
240V/50Hz			
100V/60Hz	+15V	3A	3 sec.(max)
240V/50Hz			
100V/60Hz	+9V	3A	3 sec.(max)
240V/50Hz			
100V/60Hz	+5V	3A	3 sec.(max)
240V/50Hz			

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2.5.Plug in/out Sequence

Output voltage transition sequence form 5V to 9V/15V/20V.



Note 1 : The slew rate of the positive and negative transition shall not exceed 30mv/us

Time interval	Description	PD SPEC
T0	Before ADP&KIT CC pin connected	---
T1	ADP&KIT CC pin connected,Vbus turn on delay time	100 ~ 200mS
T2	ADP N-Mos on, Vbus rising to 5V	T2 < 285mS
T3	CC pin communication	---
T4	Vbus rise to System request voltage	T4 < 285mS
T5	Vbus stable	---
T6	Cable plug out, Vbus is falling to 5V +5%(5.25V) regulation	T6 < 50mS
T7	Vbus is falling from Vsafe5V(5.25V) to Vsafe0V_max(0.8V)	T6+T7 < 100mS
T8	End	---
T4/T6	Max slew rate allowed for Positive	Rise < +30mV/us
	Negative voltage transitions	Fall < -30mV/us

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2.6. Power Supply Efficiency

20V/3.25A mode:

The adapter efficiency (watts output/watts input) shall be more than DOE:
88.00% that is the average value of 25%, 50%, 75% and 100% load.

15V/3A mode:

The adapter efficiency (watts output/watts input) shall be more than DOE:
87.73% that is the average value of 25%, 50%, 75% and 100% load.

9V/2A mode:

The adapter efficiency (watts output/watts input) shall be more than DOE:
85.00% that is the average value of 25%, 50%, 75% and 100% load.

5V/2A mode:

The adapter efficiency (watts output/watts input) shall be more than DOE:
78.70% that is the average value of 25%, 50%, 75% and 100% load.

Average Efficiency Requirement				
AC input	DC output	Requirement	Heat-up 30 minutes	Cold start
115V/60Hz & 230V/50Hz	20V/3.25A	Average	88.00%	87.00%
115V/60Hz & 230V/50Hz	15V/3A	Average	87.73%	86.00%
115V/60Hz & 230V/50Hz	9V/2A	Average	85.00%	83.00%
115V/60Hz & 230V/50Hz	5V/2A	Average	78.70%	76.00%

Note 1: Average Efficiency should be test after **B/I 30 min.**

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2.7. Tiny load & No Load Power Loss

Test condition			Design Requirement (Pin)		
AC input	DC output		heat-up 15minutes	cold start (idle on)	cold start (idle off)
115V/60Hz & 230V/50Hz	+20V	0.5W	< 1W	< 1.2W	< 1.2W
		0.25W	< 0.5W	< 0.65W	< 0.79W
115V/60Hz & 230V/50Hz	+15V	0.5W	< 1W	< 1.2W	< 1.2W
		0.25W	< 0.5W	< 0.65W	< 0.79W
115V/60Hz & 230V/50Hz	+9V	0.5W	< 1W	< 1.2W	< 1.2W
		0.25W	< 0.5W	< 0.65W	< 0.79W
115V/60Hz & 230V/50Hz	+5V	0W	< 0.15W	< 0.25W	< 0.3W

Note 1: Using the Power Meter of YOKOGAWA WT-210.

Note 2: Define the integral time and input power watt:

a. RD and DQE:

The integral time is 3 minutes, and heat-up 15minutes before test.

b. For 5V mode, the plug should be disconnected with the test tool.

2.8. Output Combine Regulation & Ripple/Noise test

Note 1: The ripple/noise voltage of the outputs shall be measured at the pins of the mating output connect.

Note 2: A high frequency 0.1μF & a electrolyte capacitor 10uF shall be used to terminate each output at the measurement point.

Note 3: The ripple frequencies greater than 1MHz shall be attenuated by the measurement system.

Note 4 : The adapter shall work normally from no load to maximum load.

Test condition			Design Requirement	
AC input	DC output		Item	Spec
90V/60Hz	+20V	0A	Ripple/Noise	<350mVp-p
			Regulation	19.5V~21V
		3.25A	Ripple/Noise	<350mVp-p
			Regulation	19.5V~21V
265V/50Hz		0A	Ripple/Noise	<350mVp-p
			Regulation	19.5V~21V
		3.25A	Ripple/Noise	<350mVp-p
			Regulation	19.5V~21V

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Test condition			Design Requirement	
AC input	DC output		Item	Spec
90V/60Hz	+15V	0A	Ripple/Noise	<350mVp-p
			Regulation	15.75V~14.25V
		3A	Ripple/Noise	<350mVp-p
			Regulation	15.75V~14.25V
265V/50Hz		0A	Ripple/Noise	<350mVp-p
			Regulation	15.75V~14.25V
		3A	Ripple/Noise	<350mVp-p
			Regulation	15.75V~14.25V
90V/60Hz	+9V	0A	Ripple/Noise	<350mVp-p
			Regulation	9.45V~8.55V
		3A	Ripple/Noise	<350mVp-p
			Regulation	9.45V~8.55V
265V/50Hz		0A	Ripple/Noise	<350mVp-p
			Regulation	9.45V~8.55V
		3A	Ripple/Noise	<350mVp-p
			Regulation	9.45V~8.55V
90V/60Hz	+5V	0A	Ripple/Noise	<350mVp-p
			Regulation	4.75-5.25V
		3A	Ripple/Noise	<350mVp-p
			Regulation	4.75-5.25V
264V/50Hz		0A	Ripple/Noise	<350mVp-p
			Regulation	4.75-5.25V
		3A	Ripple/Noise	<350mVp-p
			Regulation	4.75~5.25V

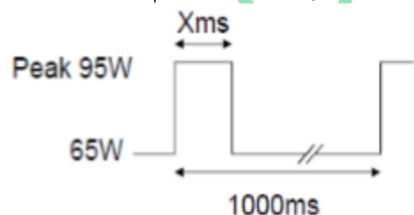
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2.9. Dynamic load

For 20V output

Test Items	Output voltage	Input voltage	Slew-rate	Test load	Lenovo Spec
Dynamic Load	20V	100Vac / 240Vac	2.5A/us	On/off= 4ms/6ms On/off=50ms/50ms Dynamic-1: 0.00A ~ 3.25A Dynamic-2: 0.20A ~ 1.50A Dynamic-3: 1.00A ~ 2.50A Dynamic-4: 1.00A ~ 3.25A	18.6V~21.4V (+/-7%)
Dynamic Load (Peak power)	20V	90Vac/47Hz 264Vac/63Hz (cold start)	2.5A/us	On/off=1m/999ms 65W-95W	18.6V~21.4V (+/-7%)

Below is Peak power test on/off time. X=1ms(Example for 20V)



For 15V output

Test Items	Output voltage	Input voltage	Slew-rate	Test load	Lenovo Spec
Dynamic Load	15V	100Vac / 240Vac	2.5A/us	0%~90% & 10%~100% On/Off=4ms/6ms, 50ms/50ms(1Hz~5kHz)	13.95V~16.0 5V(+/-7%)
Dynamic Load (Peak power)	15V	90Vac/47Hz 264Vac/63Hz (cold start)	2.5A/us	On/off=1m/999ms 45W-68W	13.95V~16.0 5V(+/-7%)

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For 9V output

Test Items	Output voltage	Input voltage	Slew-rate	Test load	Lenovo Spec
Dynamic Load(IEC requirement)	9V	100Vac / 240Vac	2.5A/us	0%~90% & 10%~100% On/Off=4ms/6ms, 50ms/50ms(1Hz~5kHz)	8.37V~9.63V (+/-7%)
Dynamic Load (Peak power)	9V	90Vac/47Hz 264Vac/63Hz (cold start)	2.5A/us	On/off=1m/999ms 27W-40.5W	8.37V~9.63V (+/-7%)

For 5V output

Test Items	Output voltage	Input voltage	Slew-rate	Test load	Lenovo Spec
Dynamic Load(IEC requirement)	5V	100Vac / 240Vac	2.5A/us	0%~90% & 10%~100% On/Off=4ms/6ms, 50ms/50ms(1Hz~5kHz)	4.1V~5.5V
Dynamic Load(Peak power)	5V	90Vac/47Hz 264Vac/63Hz (cold start)	2.5A/us	On/off=1m/999ms 15W-22.5W	4.1V~5.5V

2.10.Step Load Test

Test condition					Design Requirement
AC input	OUTPUT VOLTAGE	Load	Slew rate	On/off time	Vo
90V/60Hz & 265V/50Hz	20V	0 ~ 1A 1 ~ 2A 2 ~ 3.25A	Rise time:100us, (=Slew Rate:0.01A/uS)	0.5ms/0.5ms (1KHz)	+19.5 ~ +21V
	15V	0 ~ 1A 1 ~ 2A 2 ~ 3A			+14.25V ~ +15.75V

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Test condition					Design Requirement
90V/60Hz & 265V/50Hz	9V	0 ~ 1A 1 ~ 2A 2 ~ 3A	Rise time:100us, (=Slew Rate:0.01A/uS)	0.5ms/0.5ms (1KHz)	+8.55V ~ 9.45V
	5V	0 ~ 0.75A 0.75 ~ 1.5A 1.5 ~ 2.25A 2.25 ~ 3A	Rise :2.5A/uS Fall :2.5A/uS		+4.4V ~ +5.45V

3. Protection

3.1.Over Voltage Protection

NOMINAL OUTPUT VOLTAGE (V)	OVER VOLTAGE
	MAX.
20V	26V
15V	19.5V
9V	11.7V
5V	6.5V

The power supply is latched and power on reset is required

3.2.Over Current Protection

Test condition		Design Requirement(range)
AC input	DC output	
90V/60Hz	Auto	4.5 A max (both for 20V/15V/9V/5V)
100V/60Hz		
240V/50Hz		
265V/50Hz		

The power supply will be shut down and auto-restart.

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3.3. Short Circuit Protection

Test condition		Design Requirement
AC input	DC output	
90V/60Hz	Short output terminal of DC plug + and - .	.No damage shall occur. .Shutdown and Auto-recovery .Output RMS power < 5W
100V/60Hz		
240V/50Hz		
265V/50Hz		

The power supply will be shut down and auto-restart.

4. HI-POT test

Apply DC 4242V on primary to secondary 1sec. No component, no arcing, no noise, and the cut off current shall below 10mA.

PRI to SEC : 4242VDC (Actual Output Voltage)/1mA/1sec.

5. PD IC RT7202KF Firmware Version Confirm (use Check sum reader)

The firmware version should be confirm by **check sum reader** and the value display “0xXXXXXXXX” is stand for correct version at this stage.

(Please reference RD's mail or SR remark)

6. Output DC Plug Test

USB Type-C plug shell must be connected to ground.

PIN ASSIGNMENT	
AWG WIRE	USB PIN
Vo(RED)	A4 ,A9 ,B4 ,B9
GND(BLACK) (DRAIN+SPIRALS)	A1 ,A12 ,B1 ,B12
CC(BLUE)	A5
D+/D-	A6 ,A7 SHORTED

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