

MANUFACTURING TEST REQUIREMENT

PA-1650-88D3

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MODEL	REV	Written By	LITE-ON Electronics, Inc.
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Revision History

REV. NO.	DESCRIPTIONS OF CHANGE		Item	Change Date	REF. DOC. NO.
	BEFORE	AFTER			
A	Initial			2019/11/20	

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1. Input / Output Requirement

Input Voltage	Input Frequency
90Vac ~ 264Vac	47Hz ~ 63Hz

DC Output	MIN	MAX	UNIT
20V	0	3.25	A
15V	0	3	A
9V	0	3	A
5V	0	3	A

USB PD adapter: AC turn-on is 5V no load after PD power communication with System, power supply got system than output can support to full loading.

2. Detail Description:

2.1. Inrush Current

Test condition			Design Requirement
AC input	DC output		
115V/60Hz	+20	3.25A	REF
230V/50Hz			REF

2.2. Rated Current

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+20V	3.25A	1.7A(max)
180V/60Hz	+20V	3.25A	1.0A(max)

2.3. Power Factor

Test condition			Design Requirement
AC input	DC output		
230V/50Hz	+20V	3.25A	REF

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2.4. Turn-On Time

Test condition			Design Requirement
AC input	DC output		
90V/47Hz	+20V	3.25A	4 sec.(max)
240V/50Hz			
90V/47Hz	+15V	3A	4 sec.(max)
240V/50Hz			
90V/47Hz	+9V	3A	4 sec.(max)
240V/50Hz			
90V/47Hz	+5V	3A	4 sec.(max)
240V/50Hz			

2.5. Output Rise Time

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+20V	0A	275 mS (max)
240V/50Hz			
90V/60Hz	+15V	0A	275 mS (max)
240V/50Hz			
90V/60Hz	+9V	0A	275 mS (max)
240V/50Hz			
90V/60Hz	+5V	0A	275 mS (max)
240V/50Hz			

Note 1: Measured at CR mode from the 10% point to the 90% point on voltage waveform.

2.6. Power Supply Efficiency

Test condition			Design Requirement
AC input	DC output		
230V/60Hz	+20V	3.25A	Instantaneous Efficiency > 88%(min)
115V/60Hz	+20V	3.25A	Average Efficiency > 88.00%(min)

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230V/50Hz			
115V/60Hz	+15V	3A	Average Efficiency > 87.73%(min)
230V/50Hz			
115V/60Hz	+9V	3A	Average Efficiency > 86.62%(min)
230V/50Hz			
115V/60Hz	+5V	3A	Average Efficiency > 81.39%(min)
230V/50Hz			

Note 1: Average Efficiency for Factory CPK

Vo:20V, Average Efficiency value of 25%, 50%, 75%, 100% load condition shall be more than 86%(at cold start) with both 115Vac/230Vac.

Vo:15V, Average Efficiency value of 25%, 50%, 75%, 100% load condition shall be more than 85.73%(at cold start) with both 115Vac/230Vac.

Vo:9V, Average Efficiency value of 25%, 50%, 75%, 100% load condition shall be more than 84.62%(at cold start) with both 115Vac/230Vac.

Vo:5V, Average Efficiency value of 25%, 50%, 75%, 100% load condition shall be more than 76.5%(at cold start) with both 115Vac/230Vac.

Note 2: Full load efficiency for Factory CPK

Instantaneous efficiency value at 100% load condition shall be more than below table 87% (after B/I 30min) and 83%(at cold start) with 90Vac.

20V 87% (after B/I 30min),83%(at cold start)

15V 86% (after B/I 30min),82%(at cold start)

9V 85% (after B/I 30min),82%(at cold start)

5V 81% (after B/I 30min),79%(at cold start)

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2.7. Tiny load Power Loss

Test condition			Design Requirement
AC input	DC output		
115V/60Hz 230V/50Hz	+20V	0.25W	< 570mW (cool start)

Note 1: Using the Power Meter of YOKOGAWA WT-210.

Note 2: Define the integral time and input power watt:

- RD and DQE:
The integral time is 3 minutes, the test result should be less than input power 500mW.
- Mass production line auto-test: delay 2S, then integrate 3S.
- CPK calculation, use manual-test: delay 2mins, then integrate 3mins.
- 5V Power saving 0.25W max. For MP Line.

2.8. Output Combine Regulation & Ripple/Noise test

Note 1: The ripple/noise voltage of the outputs shall be measured at the pins of the mating output connect.

Note 2: A high frequency electrolyte capacitor shall be used to terminate each output at the measurement point (capacitor load is same as 2.9 dynamic note2).

Note 3: The ripple frequencies greater than 20MHz shall be attenuated by the measurement.

Test condition			Design Requirement	
AC input	DC output		Item	
90V/60Hz and 264Vac/50Hz	+20V	0A and 3.25A	Ripple/Noise	<600mVp-p
			Regulation	19~21V
90V/60Hz and 264Vac/50Hz	+15V	0A and 3.00A	Ripple/Noise	<450mVp-p
			Regulation	14.25~15.75V
90V/60Hz and 264Vac/50Hz	+9V	0A and 3.00A	Ripple/Noise	<300mVp-p
			Regulation	8.55V~9.45V
90V/60Hz and 264Vac/50Hz	+5V	0A and 3.00A	Ripple/Noise	<300mVp-p
			Regulation	4.75-5.25V

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2.9. Dynamic load

20V

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+18.0~+21.5V	0~3.25A	Rise: 2.5A/uS Fall: 2.5A/uS Frequency: 50Hz~10KHz
100V/60Hz			
240V/50Hz			
264V/50Hz			

Note 1: Set the load change frequency at 50Hz & 1 KHz & 10 KHz and duty at 50%.

Note 2: Add Capacitor 100uF on the load

15V

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+13.5~+16.5V	0~3.00A	Rise: 2.5A/uS Fall: 2.5A/uS Frequency: 50Hz~10KHz
100V/60Hz			
240V/50Hz			
264V/50Hz			

Note 1: Set the load change frequency at 50Hz & 1 KHz & 10 KHz and duty at 50%.

Note 2: Add Capacitor 100uF on the load

9V

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+7.8~+9.9V	0~1.5A 1.5A~3A	Rise: 2.5A/uS Fall: 2.5A/uS Frequency: 50Hz~10KHz
100V/60Hz			
240V/50Hz			
264V/50Hz			

Note 1: Set the load change frequency at 50Hz & 1 KHz & 10 KHz and duty at 50%.

Note 2: Add Capacitor 100uF on the load

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5V

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+4.3V~+5.4V	0~1.5A 1.5A~3A	Rise: 0.2A/uS Fall: 0.2A/uS Frequency: 50Hz~10KHz
100V/60Hz			
240V/50Hz			
264V/50Hz			

Note 1: Set the load change frequency at 50Hz & 1 KHz & 10 KHz and duty at 50%.

Note 2: The test need add Capacitor 100uF on the load.

Note 3: If ATE Load use 10uF / 0.1uF Cap, the 5V Dynamic spec is 3.7V~6.1V

2.10. Peak Load Test

Test condition			Design Requirement
AC input	DC output		
115V/60Hz	+20V	3.25A to 4.25A	4 sec@10%
240V/50Hz			

3. Protection

3.1. Over Voltage Protection

Test Condition			Design Requirement	
AC Input	DC Output			
90V/60Hz	+20V	3.25A	Max	Shutdown & Latch-off
240V/50Hz			26V	
90V/60Hz	+15V	3A	Max	
240V/50Hz			20V	
90V/60Hz	+9V	3A	Max	
240V/50Hz			15V	
90V/60Hz	+5V	3A	Max	
240V/50Hz			8V	

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3.2. Over Current Protection

Test Condition		Design Requirement		
AC Input	DC Output	MIN	MAX	
90V/60Hz	+20V	4.3A	6.5A	Shutdown & Latch-off
240V/50Hz				
90V/60Hz	+15V	3.5A	5.5A	Shutdown & Latch-off
240V/50Hz				
90V/60Hz	+9V	3.5A	5.5A	Shutdown & Latch-off
240V/50Hz				
90V/60Hz	+5V	3.5A	5.5A	Shutdown & Latch-off
240V/50Hz				

Note 1: After OCP occurs, the CC pin should be renegotiation.

4. HI-POT test

Apply DC 4242V on primary to secondary 1sec. No component, no arcing, no noise, and the cut off current shall below 10mA.

PRI to SEC: 4242VDC (Actual Output Voltage)/1mA/1SEC

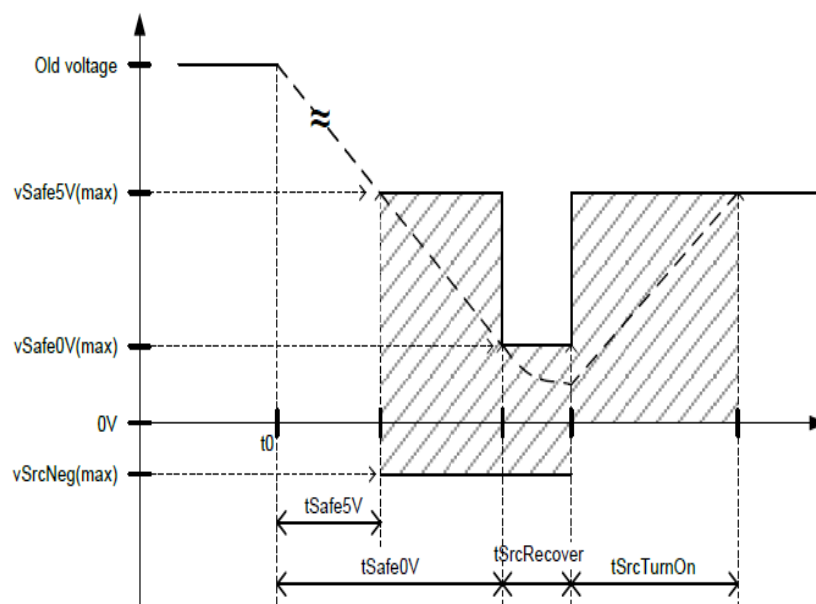
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5. Type-C and CC pin pattern test

5.1. Hard reset test for Type-C-PD adapter

The Source shall meet both *tSafe5V* and *tSafe0V* relative to the start of the voltage transition as shown in Figure 7-4.

Figure 7-4 Source V_{bus} Response to Hard Reset



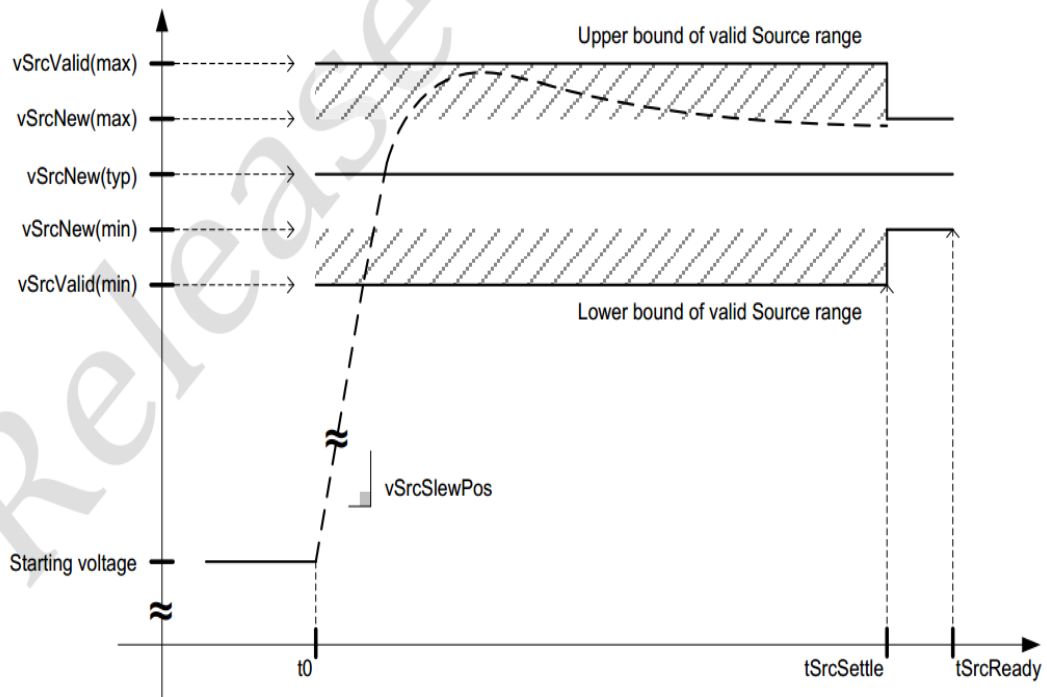
Test Condition			Design Requirement	
AC Input	DC Output			
90V/60Hz	+20V	3.25A/0A	19V-21V	tSafe5V: <275mS tSafe0V: <650mS tSrcRecover: <1S
240V/50Hz				
90V/60Hz	+15V	3A/0A	14.25V-15.75V	
240V/50Hz				
90V/60Hz	+9V	3A/0A	8.55V-9.45V	
240V/50Hz				
90V/60Hz	+5V	3A/0A	4.75V-5.25V	
240V/50Hz				

(Voltage transit duration loading will be 1A)

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5.2. Voltage transition test for Type-C-PD adapter

Figure 7-2 Transition Envelope for Positive Voltage Transitions

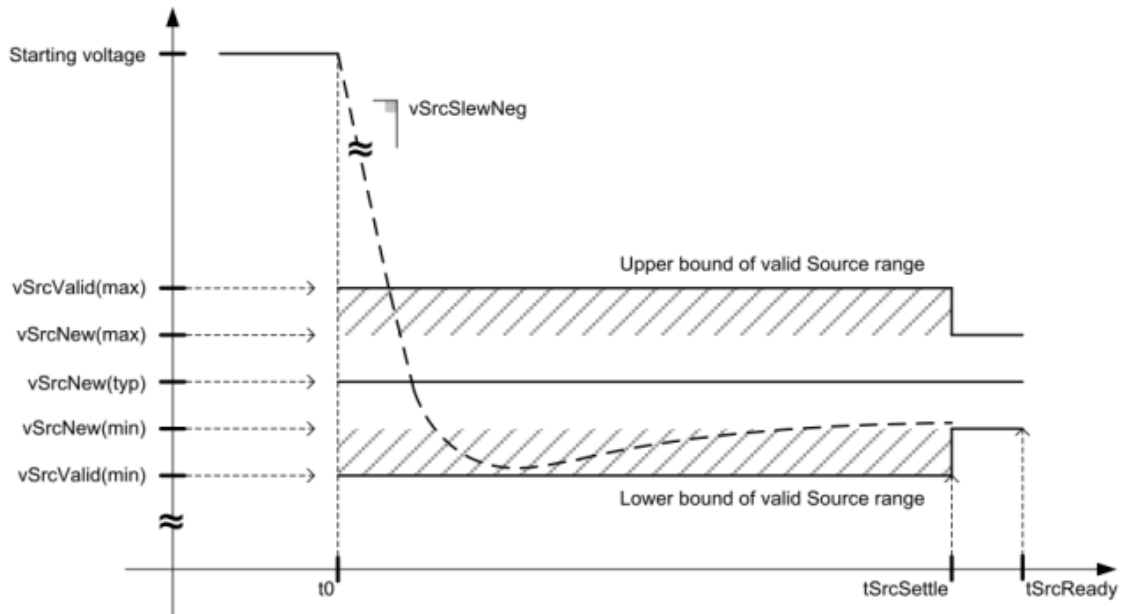


Test Condition		Design Requirement	
AC Input	DC Output		
90V/60Hz	+20V to 5V	19V-21V	tSrcSettle: <275mS tSrcReady: <285mS
240V/50Hz			
90V/60Hz	+15V to 5V	14.25V-15.75V	
240V/50Hz			
90V/60Hz	+9V to 5V	8.55V-9.45V	
240V/50Hz			

(Voltage transit duration loading will be 1A)

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Figure 7-3 Transition Envelope for Negative Voltage Transitions



Test Condition		Design Requirement	
AC Input	DC Output		
90V/60Hz	+5V to 20V	19V-21V	tSrcSettle: <275mS tSrcReady: <285mS
240V/50Hz			
90V/60Hz	+9V to 15V	14.25V-15.75V	
240V/50Hz			
90V/60Hz	+5V to 9V	8.55V-9.45V	
240V/50Hz			

(Voltage transit duration loading will be 1A)

5.3.CC pin eye pattern test for Type-C-PD adapter

Equipment : Oscilloscope : Tektronix DPO7104C

Software GRL-USB-PD version 1.2.2.0

Test critical:

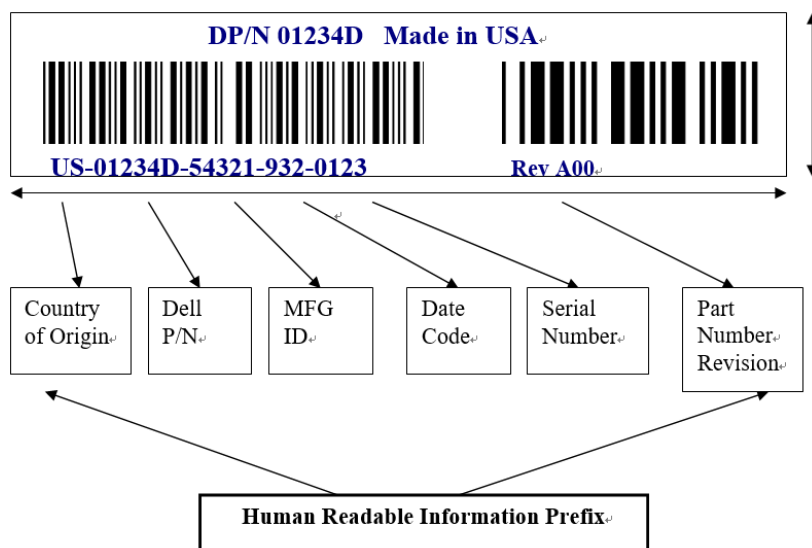
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SI No	Test Name	Test Result	Test Limit	Average Value	Minimum Value	Maximum Value
1	Eye Diagram One Mask Test	PASS	-	-	-	-
2	Eye Diagram Zero Mask Test	PASS	-	-	-	-
3	CRC Test	PASS	-	-	-	-
4	Rise Time Test	PASS	$X > 300 \text{ ns}$	373.268522 nS	344.736555 nS	379.668262 nS
5	Fall Time Test	PASS	$X > 300 \text{ ns}$	351.468439 nS	334.938233 nS	357.103077 nS
6	Symbol Encoding Test	PASS	-	-	-	-
7	Packet Format Test	PASS	-	-	-	-
8	Bit Rate Test	PASS	$(270 < X < 330) \text{ Kbps}$	296.446 Kbps	294.437 Kbps	298.265 Kbps
9	Inter-Frame Gap Test	NA	-	-	-	-
10	Unit Interval Test	PASS	$(3.03 < X < 3.70) \mu\text{s}$	3.37333849 μs	3.35272315 μs	3.39631214 μs
11	Voltage Swing Test	PASS	$(1.05 < X < 1.20) \text{ V}$	1.128 V	1.116 V	1.16 V
12	pBitRate Test	PASS	$X < 0.25 \%$	0.005 %	0.005 %	0.005 %

6. Insulation Resistance

Apply DC 500V on primary to secondary and measured the resistance shall be large than 30M ohms.

7. PPID Description



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8. PSID Checksum

PN: 8A049X / Rev: V03 / Checksum: 002C3045

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