

MANUFACTURING TEST REQUIREMENT

MODEL NO : PA-1181-28D

OUTPUT POWER : 180W

DATE : 2017/10/23

REV : A

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APPROVED BY :

REV. NO.	DESCRIPTIONS OF CHANGE		Item	Change Date	REF. DOC. NO.
	BEFORE	AFTER			
X01	INITIAL			2017/04/14	
X02	Correct table 2.3 and 3.2.			2017/05/24	
X03	Update table 2.4, 2.6, 2.7			2017/07/03	
A01				2017/09/22	
A02	Update efficiency 87% (at cold start)			2017/10/23	

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1. INPUT \ OUTPUT REQUIREMENT

Input Voltage	Input Frequency
90VAC ~ 264VAC	47Hz ~ 63Hz

NOMINAL VOLTAGE (V)	LOAD CURRENT(A)		REGULATION
	MIN.	MAX.	
19.5	0	9.23	18.5V-20.5V

2. DETAIL DESCRIPTION:

2.1 INRUSH CURRENT

Test Condition			Design Requirement
AC Input	DC Output		
115V 60Hz	+19.5V	9.23A	140A Peak (for reference) Or No function error, no damage
230V 50Hz		(Condition 1)	

2.2 INPUT CURRENT

Test Condition			Design Requirement
AC Input	DC Output		
90V 50Hz	+19.5V	9.23A (Condition 1)	≤2.34A
180V 60Hz	+19.5V	9.23A (Condition 1)	≤1.25A

2.3 POWER FACTOR

Test condition			Design Requirement
AC input	DC output		
115V/60Hz	+19.5V	9.23A (Condition 1)	0.92(min)
230V/60Hz	+19.5V	9.23A (Condition 1)	0.92(min)
115V/60Hz	+19.5V	3.692A	0.6(min)
230V/60Hz	+19.5V	3.692A	0.6(min)

2.4 HOLD UP TIME

Test Condition		Design Requirement
AC Input	DC Output	

90V 60Hz	+19.5V	7.384A	$\geq 16\text{mS}$
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2.5 TURN ON DELAY TIME

Test Condition			Design Requirement
AC Input	DC Output		
90V 47Hz	+19.5V	0A	≤3S
264 63Hz		7.3A	

Note1: A 2200PF/25V electrical capacitor shall be used to terminate output at the measurement point for turn on test;

Note2: Delay time from the AC on point to the 90% point of the output voltage.

2.6 POWER SUPPLY EFFICIENCY

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+19.5V	9.23A	Instantaneous Efficiency > 88%(min)
115V/60Hz	+19.5V	9.23A	Average Efficiency > 88%(min)
230V/50Hz			

Note1: Average Efficiency value of 25%, 50%, 75%, 100% load condition shall be more than 88% (after B/I 30min)

Note2: Instantaneous efficiency value at 100% load condition shall be more than 88% (after B/I 30min) and **87%**(at cold start) with 90Vac.

Note3: As factory manufacture procedure can't meet standard test method, manufacture procedure can use below test condition in factory.

(1)For CPK calculation Test method:

Instantaneous efficiency value at 100% load conduction shall be more than 84% at cold start.

Instantaneous efficiency value at 100% load conduction shall be more than 88% (after B/I 30min).

(2)For mass production line auto-test Test method:

Instantaneous efficiency value at 100% load conduction shall be more than 84% at cold start.

2.7 POWER CONSUMPTION

Test condition			Design Requirement
AC input	DC output		
115V/60Hz 230V/50Hz	+19.5V	0.25W	< 481mW

115V/60Hz 230V/50Hz	+19.5V	0.5W	< 943mW
115V/60Hz 230V/50Hz	+19.5V	1W	< 1.694W
115V/60Hz 230V/50Hz	+19.5V	2W	< 3.076W
115V/60Hz 230V/50Hz	+19.5V	5W	< 7.14W
115V/60Hz 230V/50Hz	+19.5V	10W	< 13.33W
115V/60Hz 230V/50Hz	+19.5V	15W	< 18.75W
115V/60Hz 230V/50Hz	+19.5V	20W	< 24.39W

Note1: Using the Power Meter of YOKOGAWA WT-210.

Note2: As factory manufacture procedure can't meet standard test method, manufacture procedure can use below test condition in factory.

(A) For **CPK** calculation Test method:

Delay 2mins, and then integrate 3mins at DC output equal to
0.25W,0.5W,1W,2W,5W,10W,15W,20W.

Design Requirement:

When Pout = 0.25W, Pin should be less than 0.481W

When Pout = 0.5W, Pin should be less than 0.943W

When Pout = 1W, Pin should be less than 1.694W

When Pout = 2W, Pin should be less than 3.076W

When Pout = 5W, Pin should be less than 7.14W

When Pout = 10W, Pin should be less than 13.33W

When Pout = 15W, Pin should be less than 18.75W

When Pout = 20W, Pin should be less than 24.39W

(B) For **mass production line** auto-test Test method: Delay 2S,
then integrate 10S.

Design Requirement:

When Pout=0.25W, Pin should be less than 0.781W

2.8 OUTPUT COMBINE REGULATION & RIPPLE / NOISE TEST

Test Condition		Design Requirement	
AC Input	DC Output	Item	+19.5V
90VAC 47Hz	0.1A, 9.23A	Ripple & Noise	<500mVp-p
		Regulation	18.50V ~ 20.5V
100VAC 60Hz	0.1A, 9.23A	Ripple & Noise	<500mVp-p
		Regulation	18.50V ~ 20.5V
240VAC 50Hz	0.1A, 9.23A	Ripple & Noise	<500mVp-p
		Regulation	18.50V ~ 20.5V
264VAC 63Hz	0.1A, 9.23A	Ripple & Noise	<500mVp-p
		Regulation	18.50V ~ 20.5V

Note1: The ripple & noise voltage of the outputs shall be measured at the pins of the mating output connector.

Note2: A high frequency 1 μ f ceramic capacitor and a 10 μ f ELE. capacitor shall be used to terminate each output at the measurement point. (Bandwidth is 20MHz)

2.9 DYNAMIC LOAD

Test condition			Design Requirement
AC input	DC output		
90V/60Hz	+18~+21V	0.05~8.307A	Rise: 0.25A/uS Fall: 0.25A/uS Frequency: 50Hz~10KHz
100V/60Hz			
240V/50Hz			
264V/50Hz			

Note1: Set the load change frequency at 50Hz & 1 KHz & 10 KHz and duty at 50%.

Note2: Output voltage overshoot and undershoot shall be less than 1.5V.

Note3: A 100 μ f ELE. Capacitor shall be used to terminate each output at the measurement point.

2.10 PEAK LOAD

The adapter shall support 12.46A to 9.23A for Ton=4000mS / Toff=36000mS at 100 ~ 240Vac and 25Deg C ambient, Vo keep in the regulation.

2.11 RISE TIME

The output rise time (measured from the 10% point to the 90% point on the waveform) shall be 2ms to 400ms at 110Vac/60Hz & 240Vac/50Hz at 7.384A(80% Load).

3. PROTECTION**3.1 OUTPUT OVER VOLTAGE PROTECTION**

Test Condition		Design Requirement		
AC Input	DC Output	Min	Max	No function error, no damage, Shutdown & latch off
100V 60Hz	+19.5V	21.2V	25V	
240V 50Hz				

3.2 OUTPUT OVER CURRENT PROTECTION**3.2.1 OVER CURRENT PROTECTION**

Test Condition			Design Requirement
AC Input	DC Output		No function error, no damage, Shutdown & latch off
90V 60Hz	+19.5V	12.6A~16A	
264V 63Hz			

Note1: the test result should meet table 3.2.2 (12.6A~16A) at cold start and Burn in 30 minute (minimum).

3.2.2 OVER CUTTENT TIME DELAY TIME

Test Condition			Design Requirement
AC Input	DC Output		30ms≤Td≤650ms
90V 60Hz	+19.5V	16A	
264V 63Hz			

Note1: The delay time (measured from output current jumped from 9.23A to 14.8A to the output voltage drop out of regulation) shall be with 30ms to 650ms.

3.3 OUTPUT SHORT CIRCUIT PROTECTION

Test Condition		Design Requirement
AC Input	DC Output	No function error, no damage, Shutdown & latch off
90V 60Hz	Short Output Terminal of the DC plug + and -.	
100V 60Hz		
240V 60Hz		
264V 60Hz		

3.4 OVER TEMPERATURE PROTECTION

When the inside temperature of PSU rise to 105~125 degree C, the PSU will shut down and latch off until the AC reset. No function error, no deformation, and no discoloration on case. Please short the RT100 to make sure the OTP circuit could work well. It simulation the over temperature condition occur.

4. HI-POT TEST

Apply AC 3kV on primary to secondary 1 min, and the cut off current shall be less than 10mA.

Hi-pot1 AC 3kV, test time 1s and Hi-pot2 DC 4242V, test time 1s.

5. PSID Regulation

Including: Family (17bytes:DELL00AC180195092) + PPID (23bytes) +Check Sum (2bytes). Total is 42 bytes.

6. INSULATION RESISTANCE

Apply DC 500V on primary-secondary for 1 min. The resistance shall be larger than 30Mohms.

7. ATE Setting.

For ATE set to avoid that input voltage (Vac) high line (180Vac~264Vac) switch to low line (90Vac~180Vac).